In the Claims:

Claim 1 (Previously presented): An apparatus of ring-back constriction, coupled to a transmission line, for constricting a ring-back effect, the apparatus comprising:

a comparator, coupled to the transmission line, for comparing a line signal on the transmission line with a reference voltage, and accordingly outputting a comparison signal;

a termination controller, coupled to the comparator, for outputting a termination control signal according to the comparison signal;

a termination variable resistor, coupled to a termination voltage and the transmission line, the resistance of the termination variable resistor being adjusted according to the termination control signal for providing a voltage to the transmission line;

a constriction controller, coupled to the comparator, for outputting a constriction signal; and

a transistor, having a gate and a source, the gate receiving the constriction signal, the transistor being coupled to a constriction voltage and the transmission line, the resistance of the transistor being adjusted according to the voltage difference between the gate and the source;

wherein when the level of the line signal changes from a first voltage level to a second voltage level, the level of the constriction signal successively changes from a

third voltage level to a fourth voltage level, maintains the fourth voltage level for a period, and returns to the third voltage level.

Claim 2 (Previously presented): The apparatus according to claim 1, wherein, when the line signal is at a high level, the resistance of the termination variable resistor is of a low value; and when the line signal transits from the high level to a level lower than the reference voltage, the comparison signal transits to low level, and then the termination controller outputs the termination control signal according to the comparison signal to change the resistance of the termination variable resistor from low value to high value.

Claim 3 (original): The apparatus according to claim 1, wherein, when the comparison signal transits from high level to low level, the resistance of the termination variable resistor begins to increase, and the resistance reaches a high value after a transition period.

Claim 4 (Currently Amended): The apparatus according to claim 1, wherein, when the line signal is at a high level, the resistance of the transistor ~~constriction variable resistor~~ is of a high value; and when the line signal transits from the high level to a level lower than the reference voltage, the comparison signal transits to a low level accordingly, then the constriction controller outputs the constriction signal according to the comparison signal to adjust the resistance of the transistor to a low value, and after the period, the resistance of the transistor transits from low value to high value.

Claim 5 (Previously presented): The apparatus according to claim 4, wherein, when the comparison signal transits from high level to low level, the resistance of the transistor transits from high value to low value, and after the delay period, the resistance of the transistor begins to rise, and reaches the high value after a transition period.

Claim 6 (original): The apparatus according to claim 1, wherein, the termination controller comprises a weak transistor and the weak transistor takes a transition period to change the resistance of the termination variable resistor from low value to high value.

Claim 7 (original): The apparatus according to claim 6, wherein the weak transistor is a PMOS transistor.

Claim 8 (Previously presented): The apparatus according to claim 1, wherein the constriction controller comprises a weak transistor and the weak transistor takes a transition period to change the resistance of the transistor from low value to high value.

Claim 9 (original): The apparatus according to claim 8, wherein the weak transistor is a PMOS transistor.

Claim 10 (original): The apparatus according to claim 1, wherein the termination variable resistor comprises a PMOS transistor.

Claim 11 (Previously presented): The apparatus according to claim 1, wherein the transistor comprises a PMOS transistor.

Claim 12 (original): The apparatus according to claim 1, wherein the reference voltage is 1 volt.

Claim 13 (original): The apparatus according to claim 1, wherein the termination voltage is 1.5 volt.

Claim 14 (original): The apparatus according to claim 1, wherein the constriction voltage is higher than the termination voltage.

Claim 15 (original): The apparatus according to claim 1, wherein the range of the constriction voltage is from 2.5 volt to 2.6 volt.

Claim 16 (original): The apparatus according to claim 1, wherein the transmission line is in a GTL+ (Gunning Transistor Logic Plus) bus.

Claim 17 (Previously presented): The apparatus of ring-back constriction, coupled to a transmission line, for constricting a ring-back effect, the apparatus comprising:

a comparator, coupled to the transmission line, for comparing the line signal with a reference voltage, and accordingly outputting a comparison signal;

a termination controller, coupled to the comparator, for outputting a termination control signal according to the comparison signal;

a termination variable resistor, coupled to a termination voltage and the transmission line, the resistance of the termination variable resistor being adjusted according to the termination control signal for providing a voltage to the transmission line;

a constriction controller, coupled to the comparator, for outputting a constriction signal, the constriction controller comprising:

a delay unit for delaying the comparison signal for a delay period;

an inverter for inverting the comparison signal; and

a NAND gate for receiving the delayed comparison signal and the inverted comparison signal and accordingly generating the constriction signal; and

a transistor, having a gate and a source, the gate receiving the constriction signal, the transistor being coupled to a constriction voltage and the transmission line, the resistance of the transistor being adjusted according to the voltage difference between the gate and the source.